* ***Comparison b/w CISC and RISC Architecture***

| **CISC** | **RISC** |
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| A large number of instructions are present in the architecture. | Very few instructions are present. The number of instructions are generally less than 100. |
| Some instructions with long execution times. These include instructions that copy an entire block from one part of memory to another and others that copy multiple registers to and from memory. | No instruction with a long execution time due to a very simple instruction set. Some early RISC machines did not even have an integer multiply instruction, requiring compilers to implement multiplication as a sequence of additions. |
| Variable-length encodings of the instructions. **Example:** IA32 instruction size can range from 1 to 15 bytes. | Fixed-length encodings of the instructions are used. **Example:** In IA32, generally all instructions are encoded as 4 bytes. |
| Multiple formats are supported for specifying operands. A memory operand specifier can have many different combinations of displacement, base, and index register. | Simple addressing formats are supported. Only base and displacement addressing is allowed. |
| CISC supports array. | RISC does not support array. |
| Arithmetic and logical operations can be applied to both memory and register operands. | Arithmetic and logical operations only use register operands. Memory referencing is only allowed by load and store instructions, i.e. reading from memory into a register and writing from a register to memory respectively. |
| Implementation programs are hidden from machine-level programs. The ISA provides a clean abstraction between programs and how they get executed. | Implementation programs exposed to machine level programs. Few RISC machines do not allow specific instruction sequences. |
| Condition codes are used. | No condition codes are used. |
| The stack is being used for procedure arguments and returns addresses. | Registers are being used for procedure arguments and return addresses. Memory references can be avoided by some procedures. |